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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,881	08/27/2002	Yi-Chen Chang	9641-US-PA	6186

31561 7590 12/27/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
EISEN, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,881	CHANG, YI-CHEN	
	Examiner	Art Unit	
	Alexander Eisen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The rejection of claim 19 under 35 U.S.C. 112(2) and the objection to a disclosure have been withdrawn in view of applicant's amendment.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 and 6-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato et al., ("Sato"), US 2002/0140645 A1.

With respect to claim 1 Sato discloses a driving method for a light-emitting device for use in an active matrix display comprising a driver circuit (data driving circuit DDR - see FIG. 1) to control the light-emitting device, the data driver circuit comprising a data input terminal (PAD1) for inputting a data signal so as to control a status of a light-emitting device; providing a clock and partitioning the clock into first clock and a second clock (see CLK+ and CLK- in FIG. 4), wherein the first and the second clock have the same frequencies but are asynchronous to each other (shifted by 180 degrees); inputting the data signal to the data inputting terminal at the first clock; and inputting the reset signal to the data terminal of the driver circuit at the second clock (see FIGS. 3, 4; paragraphs [0086-0099]).

As to claim 2, the light-emitting device includes an organic light-emitting diode ([0079]).

As to claims 3 and 4, as can be seen from FIG. 4 the frequencies of the first and the second clocks are the same, and amount to 60 Hz (paragraph [0009]).

As to claim 6, the light-emitting device includes an organic light-emitting display to construct a thin-film transistor active matrix organic light-emitting diode display.

As to claims 7 and 8, see paragraphs [0089], [0092-96] and [0101-0102]).

As to claim 9, as can be seen from FIG. 4, reset signal includes a negative signal.

As to claim 10, the reset signal enables the capacitor CPR to discharge, wherein the capacitor is used to maintain a voltage for switching a driving device (TFT2) of the driver circuit (see abstract; .

As to claim 11, see paragraphs [0034-0035] and [0083].

As to claim 12, Sato discloses a driving method for a light-emitting device including a video control unit for continuously receiving video signal with a frame as a unit (paragraph [0009]), the frame being inputted with an image display clock, the driving method comprises fixing a reset clock R (FIG. 4) after the clock control unit outputs the image signal and before the frame is changed (before the next signal ST in FIG. 4), a reset signal of a fixed frequency corresponding to the frame is output to the active matrix light-emitting display to temporarily switch off a plurality of pixel units corresponding to the frame.

As to claim 13, as can be seen from FIG. 4, the reset clock and the image display clock are spaced by approximately (synchronism is not essential for practicing the invention, see paragraph [0031] of the disclosure) half a clock of the image display clock (see also paragraph [0094]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato.

With respect to claim 16 Sato discloses a driving method for a light-emitting device for use in an active matrix display comprising a driver circuit (data driving circuit DDR - see FIG. 1) to control the light-emitting device, the data driver circuit comprising a data input terminal (PAD1) for inputting a data signal so as to control a status of a light-emitting device; providing a clock and partitioning the clock into first clock and a second clock (see CLK+ and CLK- in FIG. 4), wherein the first and the second clock have the same frequencies but are asynchronous to each other; inputting the data signal to the data inputting terminal at the first clock; and inputting the reset signal to the data terminal of the driver circuit at the second clock.

Sato teaches color display (paragraphs [0071] and [0084]) but does not disclose that a color decoding unit for extracting an image signal from the video signal and a buffer memory unit for temporarily storing an image data obtained by decoding and processing of the image signal. Color decoding and extracting an image signal from video signal and frame buffers for storing image data are notoriously known to those of ordinary skills in the art, they are inherently present in modern display systems, and it would have been obvious to one of ordinary skills in the art at the time when the invention was made to use them.

As to claims 5 and 19, Sato teaches (paragraph [0009] that field clocks are double of the frame clocks (field period is set to half of one frame period), and even thought Sato does not specifically teaches that the clock is double of the first clock (image display clock), there is no criticality of this feature for practicing the invention is shown, and therefore it would be obvious to those skilled in the art that the clock can be in simply chosen as a matter of design consideration.

As to claims 14, 15 and 18, it is well known in the art to use a common clock, whereby all other necessary synchronizing signals and clocks are derived from that common clock. Therefore, it would not be a burden to one of ordinary skill in the art at the time when the invention was made to provide clocks as in FIG. 4 of Sato using common clocks derived by partitioning the latter. It is also should be noted that there is no criticality of this features for practicing the invention is shown, and therefore it would be obvious to those skilled in the art at the time of the invention that the clock structure can be in simply chosen as a matter of design consideration as far as it satisfies the display and reset requirements.

As to claim 17, as can be seen from FIG. 4, the reset clock and the image display clock are spaced approximately (synchronism is not essential for practicing the invention, see paragraph [0031] of the disclosure) by half a clock of the image display clock (see also paragraph [0094]).

As to claim 20, it is well known in the art that most of the circuitry is realized (packaged into) using chips.

Response to Arguments

6. Applicant's arguments filed 21 September 2004 have been fully considered but they are not persuasive. Applicant argues that the period is larger than the pulse width of the clock. While examiner respectfully agrees with this statement it should be noted that the period of the clock in Sato, reference of record, is also clock larger than the width of the clock itself, and this will be true for any clocks for that matter, since the period consists of pulse period and non-pulse period and therefore is always larger than the pulse period. Applicant further argues that the first clock is used normally to display frame, while the second clock is used to discharged frames. Examiner failed to find this language in claims. Even though claim 12 cites "a fixed frequency, corresponding to the frame", such language is not explicit and it is understood that reset pulse in Sato, being synchronous with horizontal pulse (one row of the display frame) as shown in FIG. 4, will also "correspond" with frame frequency, which is a multiple of line frequency. Applicant also argues that reset in Sato is for the data signal immediately in front of data lines while reset of the invention is to "temporarily switch off the pixel units". Examiner respectfully disagrees. Data lines are fed to pixels and therefore for all practical purposes the reset of data lines can be viewed as reset of pixels. Applicant further argues that the present invention uses the reset signal to "reset the pixel unit, particularly to switching off the driving transistor 102". The transistor 102 is shown in FIG. 1, which is marked as "PRIOR ART". Even if display cell of the invention is similar to that shown in FIG. 1, there is no means provided for "discharging pixel units" per se, the only way to do it is to supply discharge data through the data line to the transistor 100. This will constitute the same arrangement as in reference of record, i.e. Sato. The rejection are maintained.

Conclusion

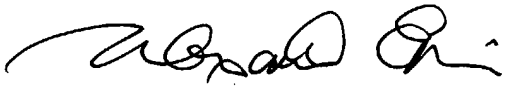
7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (703) 306-2988. The examiner can normally be reached on M-F (8:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander Eisen
Primary Examiner
Art Unit 2674

21 December 2004